IN THE SPECIFICATION:

Please amend the section title appearing directly above the paragraph that was inserted by amendment dated May 16, 2000, and immediately preceding "BACKGROUND OF THE INVENTION" as follows:

~~CROSS-REFERENCE~~ CROSS-REFERENCE TO RELATED ~~APPLICATIONS~~ APPLICATION

Please amend the paragraph bridging pages 2 and 3 as follows:

Metallic silicides have recently become popular for use as low-resistivity trace material. Tungsten silicide ("WSi_x") has become a leading low-resistivity trace material. Various etching chemistries have been developed to pattern the WSi_x to form such conductors as the digitlines or wordlines used in memory devices (see ~~commonly-owned~~ commonly owned U.S. Patent 5,492,597 hereby incorporated herein by reference). Other metallic silicides used in gate stacks include cobalt silicide ("$CoSi_x$"), molybdenum silicide ("$MoSi_x$"), and titanium silicide ("$TiSi_x$"). These metallic silicides have lower resistivity and are easier to fabricate than other conductors used for this purpose. However, metallic silicides are prone to oxidization. Furthermore, the metal components of the metallic silicides react chemically when they contact other elements. These properties present several problems, including degradation of the semiconductor element and peeling of the metallic silicide film. To compensate for these problems, a polysilicon layer is usually disposed between a gate dielectric layer and the metallic silicide film, and a dielectric cap layer is usually disposed above the metallic silicide film to isolate the metallic silicide.

Please amend the first full paragraph appearing on page 3 as follows:

FIGS. 14-19 illustrate, in ~~cross-section,~~ cross-section, a conventional method of forming a gate stack having a metallic silicide film layer. FIG. 14 illustrates a gate dielectric layer 204 such as silicon dioxide (SiO_2) grown (by oxidation) or deposited (by any known industry standard technique, such chemical vapor deposition or the like) on a silicon substrate 202. A polysilicon layer 206 is formed on top of the gate dielectric layer 204, as shown in FIG. 15. The

polysilicon layer 206 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 16, a metallic silicide film 208 is deposited on the polysilicon layer 206. The structure 118 is then subjected to a heat treatment for about 30 minutes at a temperature between about ~~850°~~ 850°C and 950°C for activation of the impurities in the polysilicon layer 206 and to anneal the metallic silicide film 208. The heat treatment temperature level is dictated by the temperature required to anneal the metallic silicide film 208. The annealing of the metallic silicide film 208 is used to reduce its resistivity.

Please amend the first full paragraph appearing on page 5 as follows:

Metallic silicides are generally represented by the formula "MSi_x" wherein: "M" is the metal component (i.e., cobalt ~~"Co",~~ "Co," molybdenum ~~"Mo",~~ "Mo," titanium ~~"Ti",~~ "Ti," tungsten ~~"W",~~ "W," and the like), "Si" is silicon, and "x" is the number of silicon molecules per metal component molecule ("x" is usually between about 2 and 3). Metallic silicide films tend to peel when a low ratio of silicon to metal component is used for gate stack formation (e.g., when "x" is less than 2). In order to reduce the stress of metallic silicide film which causes peeling, a silicon rich metallic silicide film is used in gate stack formation. In particular with the use of WSi_x, an "x" of about 2.3 is preferred.

Please amend the second full paragraph appearing on page 6 as follows:

In a preferred variation of the method, the dielectric cap is selectively deposited on an upper surface of the metallic silicide film at low temperatures. The dielectric cap material is preferably silicon nitride. The deposition of the silicon nitride layer is carried out at between ~~about 400~~ about 400°C and 600°C, which temperature does not anneal the metallic silicide film, and thus does not result in the growth and formation of silicon clusters in the metallic silicide film. It is, of course, understood that the cap can include silicon dioxide layers, or the like, so long as deposition is performed at temperatures below about 600°C. Forming the cap by selectively depositing silicon nitride by plasma-enhanced chemical vapor deposition ("PECVD") is also preferred, since only one surface of the substrate is covered by the dielectric material

which eliminates the necessity of removing the cap material from the semiconductor substrate back surface, thus providing a process cost advantage.

Please amend the second full paragraph appearing on page 7 as follows:

It is, of course, understood that if a lower resistivity in the metallic silicide is required for a specific application, the gate stack can be subjected to a heat cycle after gate stack etching to anneal the metallic silicide in the gate stack. However, if the gate stack is annealed after formation, the anneal temperature must be increased by ~~about 30~~ about 30°C to 50°C to achieve the same resistivity.

Please amend the paragraph bridging pages 8 and 9 as follows:

FIGS. 1-6 illustrate a method, in ~~cross-section,~~ cross-section, of forming a gate stack of the present invention. FIG. 1 illustrates a gate dielectric layer 104 such as silicon dioxide formed on a silicon substrate 102. A polysilicon layer 106 is formed on top of the gate dielectric layer 104, as shown in FIG. 2. The polysilicon layer 106 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 3, a metallic silicide film 108 is deposited on the polysilicon layer 106. The metallic silicide film can be deposited by CVD (including LPCVD, APCVD, and PECVD), sputtering, or the like.

Please amend the first full paragraph appearing on page 9 as follows:

A cap 110, preferably including silicon nitride, is then deposited on the metallic silicide film 108, as shown in FIG. 4. The deposition of the silicon nitride layer is carried out at between ~~about 400~~ about 400°C and 600°C, and preferably at about 500°C, by CVD (including LPCVD, APCVD, and PECVD), sputtering, spin-on techniques, or the like. In a preferred embodiment, the deposition of the silicon nitride is accomplished by plasma-enhanced chemical vapor deposition. It is, of course, understood that the cap 110 can include other dielectric material such as silicon dioxide, as long as it deposited at temperatures below about 600°C.

Please amend the third full paragraph appearing on page 9 as follows:

FIGS. 7-13 illustrate an alternate method, in ~~cross-section,~~ cross-section, of forming a gate stack of the present invention. The steps of the alternate method are similar to the method illustrated in FIGS. 1-6; therefore, components common to both FIGS. 1-6 and FIGS. 7-13 retain the same numeric designation. FIG. 7 illustrates a gate dielectric layer 104 grown or deposited on a silicon substrate 102. A polysilicon layer 106 is formed on top of the gate dielectric layer 104, as shown in FIG. 8. The polysilicon layer 106 is then subjected to an ion implantation with gate impurities (not shown). As shown in FIG. 9, a metallic silicide film 108 is deposited on the polysilicon layer 106. A cap 110 is then deposited on the metallic silicide film 108, as shown in FIG. 10. The structure 118 is subjected to a heat cycle either to anneal the metallic silicide film 108 prior to depositing the cap 110, to form the cap 110 with a high temperature process (i.e., over 600°C), or both, such that silicon clusters 116 are formed in the metallic silicide film 108.